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Optimization of FinFET's Fin Width and Height with Self-heating Effect

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***Abstract*—In this paper, we investigated the optimization of the fin width and height with an effective width of 40 nm under the conditions considering self-heating effect (SHE) through TCAD simulation. To ensure the reliability, calibration is performed with transfer curves based on experimental data. We demonstrate the region of device characteristic inversion caused by the difference in thermal resistance based on the variation in the area of heat dissipation for various fin widths. As a result, it is found that a fin width of 10 nm, which is neither too narrow nor too wide, is less affected by SHE.**

***Index Terms*—FinFET, SHE, Lattice temperature, thermal conductivity, thermal resistance**

I. INTRODUCTION

The advancement of semiconductor process technology enables the design of integrated circuits and leads to scaling down of metal-oxide-semiconductor field effect transistor (MOSFET) for better performance and higher integration density [1]. However, MOSFET has the side effects such as short-channel effects (SCEs) and reliability issues by scaling down. To retain the reliability of device and overcome the SCEs, the multi-gate FETs such as FinFET have been developed for the advanced technology nodes [2]. FinFET has great control on SCE as it is surrounded by gate from three sides [3, 4]. FinFET structures can suppress the SCEs and improve the device performance [5]. By these advantages, FinFET technology has been improved and applied in lots of products. Even though FinFET has good performance, the reliability issues have been reported. In particular, self-heating effect (SHE), which deteriorates the thermal characteristics and electrical performance [6, 7], is emerging as the modern structures are adapted. Therefore, the studies about the effect of the SHE on the FinFET is needed. The SHE can cause the degradation in carrier mobility by lattice scattering [8]. It results the decrease in on current (I_{on}) and transconductance (g_m) by scaling down and application of FinFET [9, 10]. In addition, the SHE causes the side effects such as the hot carrier injection effect (HCI), metallization lifetimes of circuit and negative-bias temperature instability (NBTI) [11-13]. The SHE comes from the lowered thermal conductance in device [14]. The major factors influencing the thermal characteristics are the thermal conductivity and the device dimension. Especially, FinFET structure has lower thermal conductance compared to planar structure, as the fin is surrounded by the gate dielectric materials such as SiO_2 (1.4 W/m·K) and HfO_2 (2.3 W/m·K) which have the lower thermal conductivity than Si (25 W/m·K) [15, 16]. Therefore, considering the higher thermal conductance of device is desired to suppress the SHE [17, 18]. However, it is very challenging to alternate the materials with high conductivity. Therefore, the fin dimension modulation is considered to ensure the higher

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thermal conductance. In addition, it is necessary to consider that the fin dimension also affects the electric characteristics. The narrower fin width can reduce the subthreshold swing (SS) and SCEs [19]. But it results the increase of source/drain resistance as the narrower fin width [20]. In conclusion, the narrower fin width has the better current characteristics [21, 22]. However, thermal conductance decreases as the fin width becomes narrow. Thus, it needs to investigate the side effect of narrowing the fin width, SHE, and optimize the fin width and height ratio to suppress the SHE and improve the device performance in both current and thermal characteristics.

To increase the current of FinFET, the effective width extension can be considered. To extend the fin width or height can be considered. However, if the fin width is extended, the device performance degrades, and if the fin height increases, there are restrictions on the process. Therefore, the multiple FinFETs are operated in parallel to increase the current [23]. For the multiple FinFETs, it is important to optimize the electro and thermal characteristics of the device.

In this study, we split the fin width and height to investigate the trade-off between the SHE and the device performance. The current degradation was compared in each structure for the presence or absence of the SHE. The narrower fin width with a little current degradation can have the best performance while managing thermal characteristics. The fin effective width is fixed at 40 nm to compare at the same W_{eff} and L ratio. The examples of FinFET which effective width is fixed at 40 nm and the split of fin width and height is shown in Fig. 1(c). The 3D schematic of FinFET is described in Fig. 1(a). For the structure of device, bulk FinFET is adopted to ensure the heat dissipation path showed as the heat flux concept diagram in Fig. 1(b). The generated heat at drain side can be diffused to bulk side [24]. By using bulk FinFET, it can verify the distinct difference about thermal conductance.

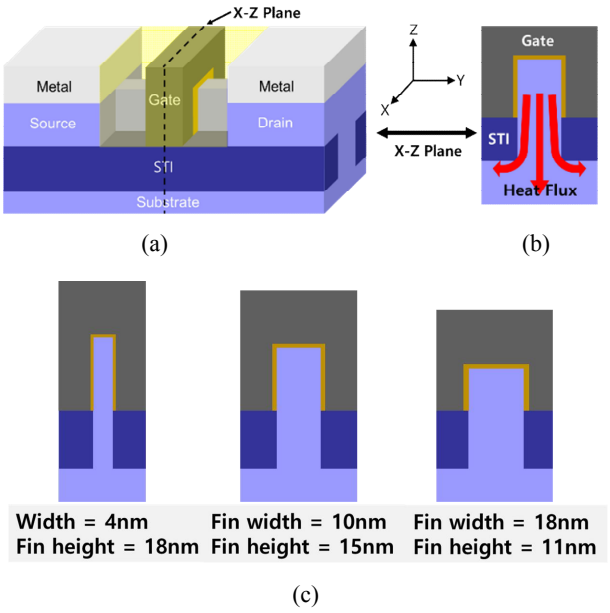

Fig. 1. (a) 3D schematic of FinFET simulated in TCAD; (b) Heat flux in the cross section of FinFET; (c) The examples of a cross section of FinFET which effective width is fixed at 40 nm.

II. Simulation Setup And Calibration

In this research, since it is difficult to measure the SHE in nanoscale, study was performed by 3D technology computer-aided design (TCAD) simulation tool, Synopsys Sentaurus [25]. Fig. 2(a) shows the overall analysis process in this research. To obtain the reliability of the simulation, the device with the same electric and thermal characteristics are analyzed through the current matching of actual FinFET data. Intel's 14 nm node bulk FinFET is adopted for the reference device which fin effective width is 92 nm [26]. To ensure the same performance through the simulation, the calibration is performed as shown in Fig. 2(b) which has good matching with the reference data. To evaluate the thermal characteristics, not only the current calibration but thermal calibration is significant. Therefore, thermal resistance calibration is performed as shown in Fig. 2(c) which reference device is SOI-MOSFET which channel length is 45 nm and normalized thermal resistance is 102.4×10^3 μm·K/W [27]. It also shows good matching with reference data.

The various mobility models are adopted such as phumob and Enormal (Lombardi) to consider coulomb, phonon and surface roughness scattering. In addition, for better accuracy, the nonlocal band-to-band tunneling (BTBT), Shockley-Read-Hall recombination (SRH), avalanche breakdown and quantum potential models are also adopted. To compare the thermal characteristics of SHE on and SHE off, the thermodynamic and the Fermi models are adapted for each simulation. Table 1 shows the parameters and geometries of the FinFET structure

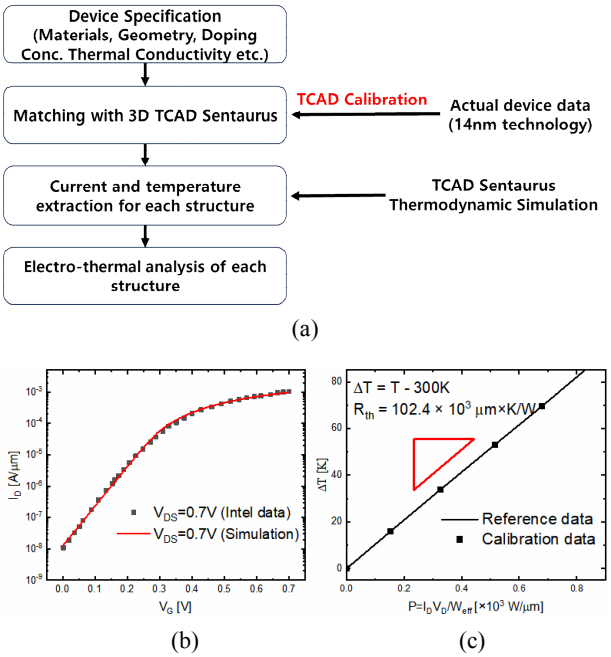

Fig. 2. (a) Workflow for the analysis of bulk FinFET under each structure; (b) Calibration curve of 14nm FinFET with experimental data; (c) $\triangle T$ vs. Power consumption per effective width of FinFET.

Table 1. Device parameters for simulation

Parameter	Value
Channel length	20 nm
Effective width	40 nm
EOT	0.5 nm
Source/Drain length	50 nm
Length of sidewall	10 nm
Gate dielectric	22 nm (HfO_2)
Spacer dielectric	7.5 (Si_3N_4)
Channel concentration	10^{15} cm^{-3}
Substrate concentration	10^{18} cm^{-3}
Source/Drain concentration	10^{21} cm^{-3}

[28]. To compare the current and thermal characteristics for the fin width and height ratio, we split the fin width and height into five kinds which the effective width is fixed at 40 nm. For each structure, transfer curve is extracted and compared about SHE on and SHE off. The thermal analysis is also performed to analyze the thermal characteristics by using the thermodynamic simulation.

III. Results And Discussion

Fig. 3(a) and (b) present the thermal characteristics of two devices with Fin widths of 4 nm and 18 nm,

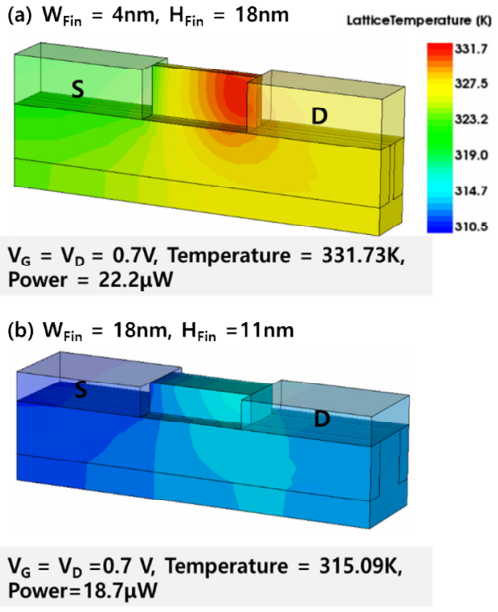

Fig. 3. Finfet lattice temperature at V_G = V_D = 0.7 V: (a) W_{fin} = 4 nm, H_{fin} = 18 nm; (b) W_{fin} = 18 nm, H_{fin} = 11 nm.

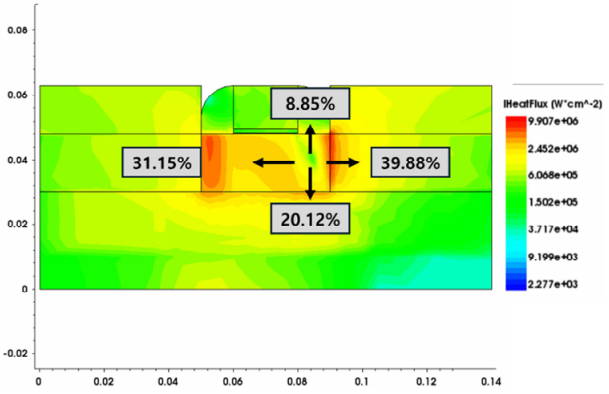

Fig. 4. The heat flux of the device at W_{fin} = 4 nm, H_{fin} = 18 nm.

respectively. The highest temperatures were measured near the top of the drain and channel regions. Applying a voltage of 0.7 V to both the gate and drain in each structure, the power consumption and heat generation were measured. In Fig. 3(a), lattice temperature of 331.73 K is measured, while Fig. 3(b) for the wider fin width showed a significantly lower temperature of 315.09 K. Fig. 4 shows the heat flux and diffusion rate for the device with fin width of 4 nm. The heat generated in channel at the drain side is diffused towards the source, drain, gate and substrate side. The heat flux toward the gate is the smallest at 8.85 % and toward the drain is the largest at 39.88 %. The others of 51.27 % are diffused to the source and substrate sides along the Si fin. This is

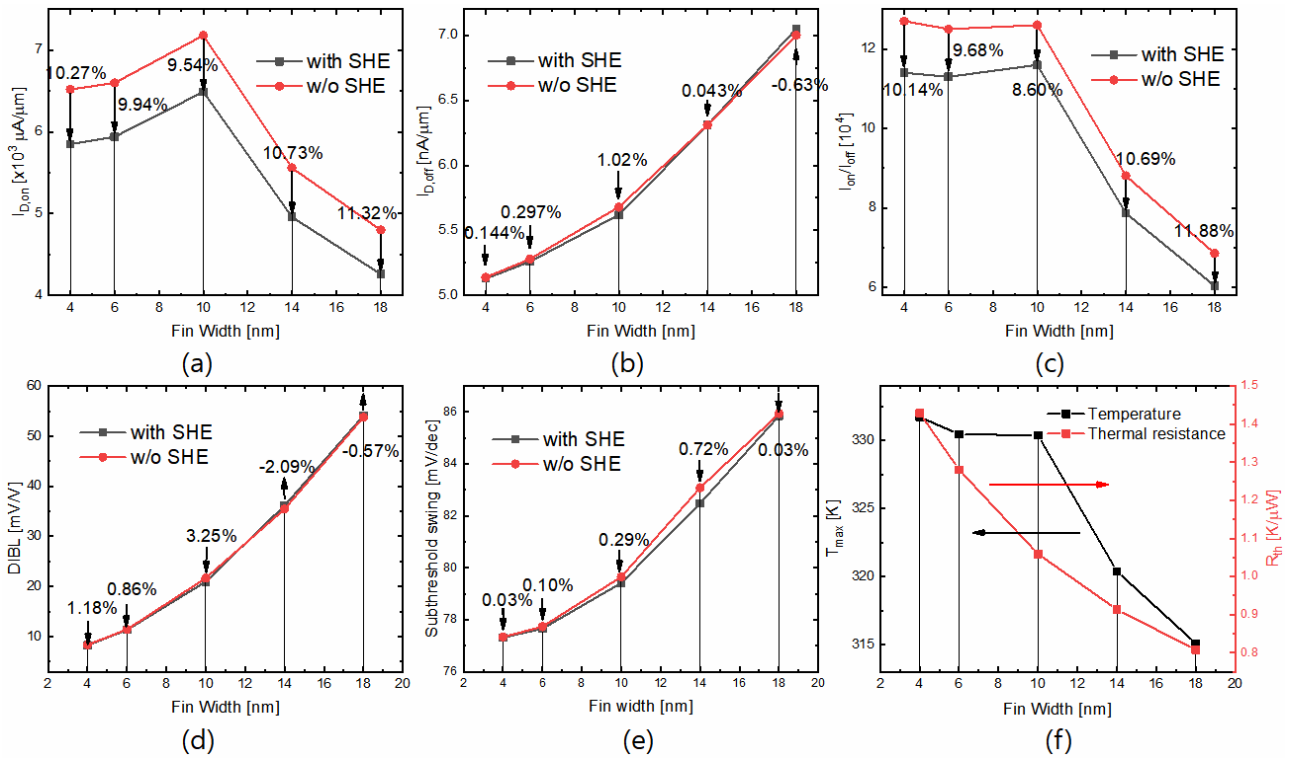

Fig. 5. Variation of output parameters of FinFET under various fin width: (a) I_{on}; (b) I_{off}; (c) on-off current ratio; (d) DIBL; (e) Subthreshold swing (SS); (f) R_{th} and lattice temperature.

primarily due to the significantly higher thermal conductivity of HfO_2 compared to Si. Therefore, the area from the drain to the source and substrate sides is a major factor in the thermal characteristic. Referring to Fig. 3 and 4, it is evident that the wider path through which heat is diffused to the substrate from the drain, the more efficient heat dissipates. Upon comparing Fig. 3(a) and (b), the narrower heat dissipation path in the Fig. 3(a) structure resulted in a higher measured lattice temperature due to its short width. To make a more accurate comparison, thermal resistance was extracted. As the Fin width increased, thermal resistance decreased, indicating improved heat dissipation. This aligns with the detailed explanation referred in Fig. 5.

To compare the I_{on} for different fin widths, V_{th} normalization was carried out by the gate overdrive 0.5 V. In Fig. 5(a), as the fin width increases from 4 nm, the I_{on} increases and has a peak value at 10 nm, then decreases and has the lowest I_{on} value at 18 nm. The narrower the fin width, the better the gate controllability as it forms a fully depleted fin, which should increase I_{on}, but the peak I_{on} at 10 nm can be explained by the quantum confinement effect. Given that our devices operate at the nano scale, the quantum confinement effect becomes influential [29, 30]. Fin widths of 4 nm and 6 nm, being devices with dimensions less than 10 nm, exhibit vulnerability to the quantum confinement effect which makes the band-gap wider, resulting in a reduction in current. We also investigated the impact of the SHE at device. Case of the fin width of 10 nm demonstrates the lowest decrease at 9.54 % with SHE. In Fig. 5(a), for fin widths of 4 nm and 6 nm, the area for the dissipation of heat is restricted. Therefore, in devices with fin widths less than 10 nm, the influence of SHE deteriorates device characteristics.

For devices with fin widths larger than 10 nm, heat dissipation is more effective, but the lower gate controllability in this case results in a significant impact even with a small amount of heat. Fig. 5(b) reveals a monotonic trend in I_{off} under difference of the fin width regardless of SHE. In the process of extracting the I_{off} from this graph, we normalized the threshold voltage of each of the five FinFET configurations in the process of extracting the I_{off} from the graph. Consequently, the I_{off} of the device is significantly influenced by the trend of subthreshold swing (SS). SS was extracted as the voltage

difference at the points where the I_{off} values were 0.9 nA/μm and 9 nA/μm. Examining the Fig. 5(e), smaller fin width results in lower SS values. Similarly, in the same context, the I_{off} also decreases with narrower fin width. We also investigated the impact of the SHE at device. For all cases except fin width 18 nm, the I_{off} decreases when SHE is on. Furthermore, in the case of a fin width of 10 nm, the most significant reduction was observed. However, the magnitude is around 1 %, and the quantitative value is on the order of nA/μm, indicating an extremely minimal effect. Even though with SHE on, the phenomenon occurs due to the lattice temperature converging to nearly 300 K under the conditions of V_G = 0 V and V_D = 0.7 V.

To compare on-off current ratio, Fig. 5(c) was extracted as the ratio of I_{on} and I_{off} normalized by V_{th}. In the case of SHE off, the 4 nm fin width device had the highest on-off current ratio, but in the SHE on case, the 10 nm device exhibited the highest ratio, reversing the trend. The degradation because SHE at fin width of 10 nm was minimal and creating a region of reversal in the quantified characteristic values. For fin width larger than 10 nm, both the quantified values of the on-off current ratio and the device degradation by SHE worsened. To compare DIBL, we applied drain voltage of 0.7 V and 0.05 V, respectively, and extracted V_{th} using the constant current method. The quantitative values of DIBL increased as fin width expanded, primarily influenced by gate controllability. We investigate the impact of SHE on the device. In Fig. 5(d), fin widths below 10 nm improve the DIBL characteristics, especially with a 3.25 % performance enhancement at 10 nm. In contrast, for 14 nm and 18 nm devices, the DIBL characteristics deteriorated. The narrower fin width, the higher lattice temperature is generated, due to lower thermal conductance. It is shown at Fig. 5(f). At the narrowest width, 4 nm, shows the highest lattice temperature of 332 K. At thermal resistance, it is higher when the dimension has the narrower fin width. It is remarkable that the fin width at 10 nm has similar lattice temperature with 6 nm, but it has the lower thermal resistance. Despite the presence of higher current drive, the wider area towards the source and substrate results in lower thermal resistance, allowing for maintaining a similar lattice temperature. In particular, considering that multiple FinFETs are operated in parallel to increase the current level., it is important to optimize the electro and thermal characteristics of device. Therefore, the device with 10 nm fin width has the most efficient thermal characteristics. It is important to adopt the proper fin width considering thermal characteristics induced by the SHE.

IV. CONCLUSIONS

The current and thermal characteristics of the FinFET were investigated by varying the fin width. By decreasing the fin width, the device performance such as subthreshold swing is improved. However thermal resistance increases resulting the increase of the lattice temperature as narrower fin width disturbs the heat to be diffused to source and substrate side. In particular, considering that multiple FinFETs are operated in parallel to increase the current level, it is important to optimize the electro and thermal characteristics of device. In this research, fin width with 10 nm shows the best performance. It is necessary to adopt the proper fin width considering thermal characteristics induced by the SHE.

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