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Analysis and Prediction of Nanowire TFET's Work Function Variation

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***Abstract*—The research investigates the electrical effect of Work Function Variation (WFV) in Tunnel Field-Effect Transistors (TFETs), with Titanium Nitride (TiN) gate as a common Metal Gate material. Employing advanced Machine Learning (ML) techniques, this study seeks to establish causal relationships among various parameters, optimize ML models, and predict exceptional scenarios. Through an in-depth analysis of diverse data, the study uncovers insights into TFET's performance variations. The ML model was optimized using the elimination method, checking each R^2 value. After discovering the relevant output parameters (e.g., turn-on voltage (V_{on}), threshold voltage (V_{th})), it was observed that WFV at particular gate regions heavily affects current variation. Furthermore, ML demonstrated the ability to predict output parameters for exceptional cases, not present in the training data, such as gates composed of the 4.4-eV grain, which exhibited a high R^2 value (0.9927).**

***Index Terms*—Machine learning, TFET, tunneling, band to band tunneling**

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I. INTRODUCTION

Recently, Tunnel Field-Effect Transistors (TFETs) have been studied as promising alternatives to metal-oxide-semiconductor field-effect transistors (MOSFETs) [1-6], particularly for very low-power application. Based on carrier injection through band-to-band tunneling (BTBT), significant progress has been made in achieving a subthreshold swing (SS) of less than 60 mV/dec at room temperature (RT) and minimizing low-level off-state current (I_{off}). Nevertheless, in contrast to MOSFETs, TFETs face a challenging issue with low on-state current (I_{on}). To address this, a high-κ / metal gate (HKMG) materials have been adopted instead of polysilicon gate. The HKMG, capable of reducing gate leakage and ensuring high channel controllability, has shown promise in improving TFET performance [7-10].

Despite advancements in I_{on} characteristics, Titanium Nitride (TiN), a common HKMG material, introduces work function variation (WFV). Sputtered TiN tends to crystallize predominantly in <200> (60%) and <111> (40%), corresponding to WFs 4.6 eV and 4.4 eV respectively. This non-uniformity in metal gates contributes to WFV, influencing TFET current variations [11-13].

Table 1. Parameters of structure

Parameters	Value
Source doping concentration (N_s)	10^{20} cm^{-3} (p-type)
Drain doping concentration (N_D)	10^{20} cm^{-3} (n-type)
Body doping concentration (N_B)	10^{18} cm^{-3} (p-type)
Gate work-function	Variable
Channel length (L_{ch})	20 nm
Channel diameter (d_{ch})	20 nm
Average metal grain size	5 × 5 nm^2
Gate oxide thickness (T_{ox})	1 nm
Drain Voltage (V_D)	1 V

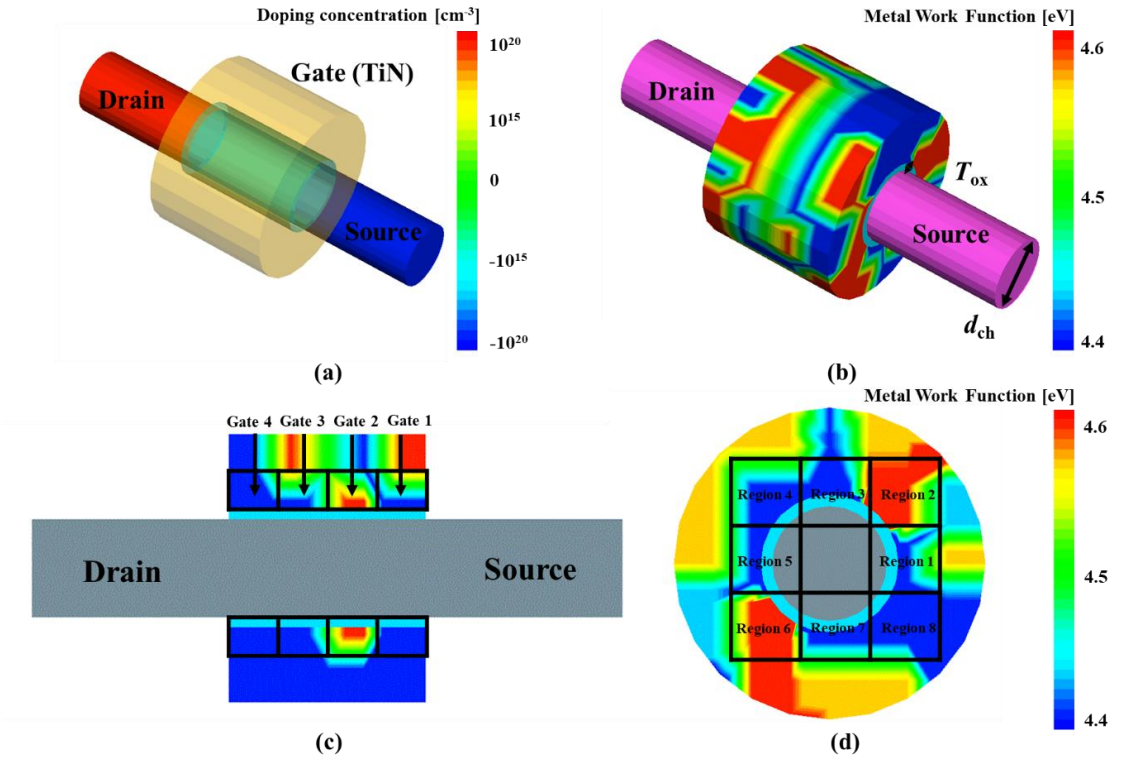

Fig. 1. (a) Bird's eye view of nanowire TFET; (b) Structure having random WF on gate; (c) Y-axis cross section and divided gate area; (d) Z-axis cross section and divided gate area.

Therefore, when implementing the TFETs into real complementary metal-oxide-semiconductor (CMOS) circuits, it is essential to examine electrical performance variations in relation to WFV. However, studies addressing this issue have been limited. Some researchers have proposed nanowire TFETs as the gate of nanowire TFET effectively reduces WFV by minimizing the affected channel area [14-16]. Despite efforts to improve this aspect, WFV still persists. Consequently, identifying the primary cause has become crucial for reducing or eliminating WFV [17].

The primary objective of this study is to establish causal relationships using a machine learning (ML) approach [18-20]. ML facilitates a comprehensive analysis of TFETs even in the absence of complete WFV data samples. It allows for predictions by adjusting output parameters and constructing a model that captures variations in electrical operations associated with WFV, combining the variation of current.

ML allows to identify the cause with a limited dataset. However, once relevant parameters are identified, ML models need optimization by pinpointing exceptional cases that were not part of the training data. Models, trained on less data tend to exhibit low R^2 value for parameters with less relevance. Therefore, it was necessary to reduce sensitivity to identify parameters that have a direct impact.

Transistor samples have been verified using technology computer-aided design (TCAD) and simulations were conducted using Synopsys Sentauraus [20, 21]. With relevant parameters, ML predicts exceptional situations by different WF in each area. In Section 2, we delve into the valuable output parameters (e.g., SS, Threshold voltage (V_{th}), minimum current (I_{min}), turn-on voltage (V_{on})) influenced by WFV. Section 3 outlines the most relevant input parameter identified by ML. Subsequently, in Section 4, the ML model is constructed using data highly dependent on Drain Voltage (V_d). Finally, Section 5 presents predictions for exceptional situations.

II. Device Design and Methodology

In Fig. 1(a), a bird's eye view of a nanowire TFET is presented. The simulation, conducted using TCAD, features a gate oxide thickness (T_{ox}) of 1 nm with SiO_2.

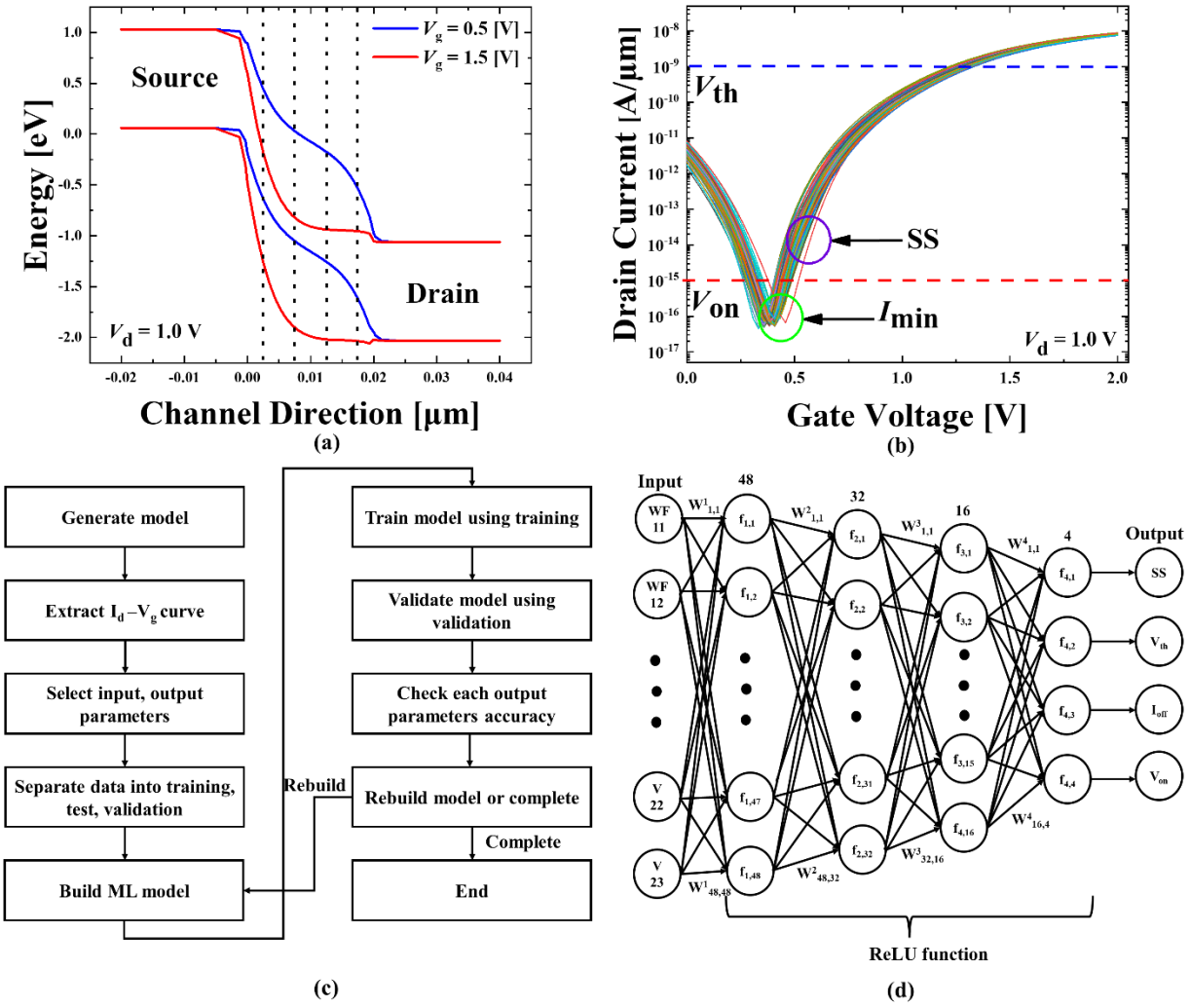

Fig. 2. (a) Energy band diagram at V_g = 0.5 V and V_g = 1.5 V; (b) I_d-V_g curve at V_d = 1.0 V; (c) Summary of ML model; (d) Visualization of ML algorithm.

Arsenic and boron are used as the dopant atoms for n-type and p-type doping, respectively. The structure of the TFET is p-i-n, with a TiN gate and a channel length of 20 nm. All simulations are performed at RT and the design parameters are summarized in Table 1. Fig. 1(b) displays a bird's eye view of a WF randomized model, while Fig. 1(c) illustrates the Y-axis cross-section. The grain size of TiN is assumed to be an identical, forming a 5 × 5 nm^2 of square shape [22].

Fig. 1(d) shows Z-axis view, where the gate covering channel is divided into 8 areas that contact the oxide part. Given the 5 × 5 nm² square shape of the TiN grain, the gate area is further divided into 32 units. WFV for each gate area is randomly assigned, taking into account these probabilities.

A thousand structures were generated for ML, with 32 WF parameters extracted from each grain near the gate. Additionally, 16 parameters, including conduction band and valance band electron volt values at V_g = 0.5 V, V_g =1.5 V, were employed to describe the WFV profile in nanowire TFET in Fig. 2(a). The parameter mark points contact with the dotted line on the graph (0.025, 0.075, 0.125, 0.175 μm). In total, 48 parameters were used for input to train the ML model.

For the ouput, four parameters (SS, V_{th}, I_{off}, V_{on}) were extracted from the I_d-V_g curve in Fig. 2(b). This curve illustates current's variation with gate voltage. I_{min}, the minimum current flowing through the device, is measured at the lowest value of drain current, marked by green circle. SS, the subthreshold swing, represents the slope with increasing current and is measured at the point where the current increases 100 times from I_{min}, indicated

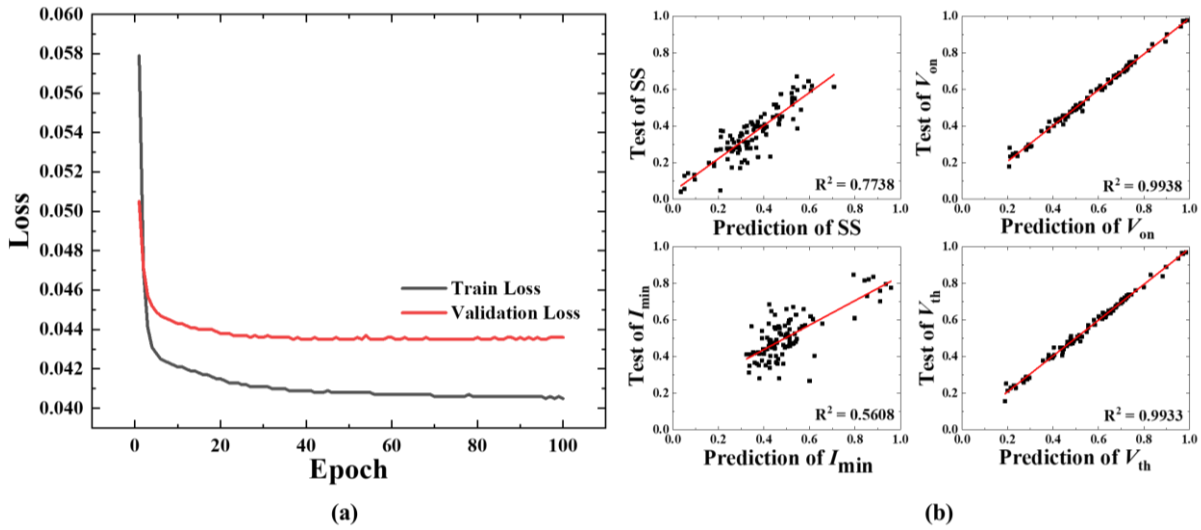

Fig. 3. (a) Loss of ML model from each epoch; (b) R^2 value of each output parameters.

by the purple circle. V_{on} is the gate voltage value defining the on-state, measured when the drain current reaches 10^{-15} A/μm marked on the blue line. V_{th}, the voltage at which the device operates, is measured when the drain current reaches 10^{-9} A/μm indicated on the red line. Its distribution follows a Gaussian distribution due to randomized grain.

To design an ML algorithm and enable predictions, the process followed the four steps, as illustrated in Fig. 2(c):

Step 1: Split the data into training, testing, and validation sets.

Step 2: Construct an ML algorithm by training it with the designated data.

Step 3: Monitor the epoch and loss until the weights are optimized.

Step 4: Adjust or refine the neural network architecture as needed and deploy it accordingly.

Following the outlined procedure, thousands of data points were divided into the ratio of 8:1:1 for training, testing, and validation. The built-in ML algorithm utilized a dense layer structure of 48 - 32 - 16 - 4 [23]. MinMaxScaler was employed to normalize parameters, ensuring consistency with the formula (i.e., $(X - X_{min}) / (X_{max} - X_{min})$). Categorical Cross-entropy served as the loss function for each dense layer in Fig. 2(d), while the Adaptive Moment Estimation (ADAM) optimizer was chosen for accurate error correction, with a learning rate (LR) set to 0.001 [24]. Fig. 3(a) depicts the loss of the ML model during the building process. The appropriate epoch, indicating the point at which the loss reaches 0.04136, was determined through the observation of loss size as the epoch increased. For quantitative correlation verification, R^2 values were extracted for various parameters. R^2 values, a statistical measure of fit, were checked for each parameter—SS (0.7738), V_{th} (0.9933), I_{min} (0.5608), and V_{on} (0.9938), as shown in Fig. 3(b).

Comparing the R^2 values for each parameter reveals a strong correlation between WFV and $V_{th,}$, V_{on}, while the relationship with I_{min} and SS is less shown. V_{th} and V_{on} exhibit higher R^2 values than SS and I_{min}. With sufficient data, the model could approach an ideal state for predicting all parameters accurately.

III. Finding the Detailed Cause

Building upon the findings in Section 2 regarding the association between WFV, V_{on}, and V_{th}, mitigating the impact on WFV has become a key focus. In TFET, V_{on} is influenced by a current at the point where BTBT is maximized. To identify a more valuable input parameter, it is essential to locate the area with maximized BTBT. In Fig. 1(c), the gate is segmented into four areas designated as gate 1, 2, 3, and 4 from the source (far right) of the structure. To assess the impact of each gate region on V_{on} using ML, two gates were grouped together. These groups of the gates served as the input for the ML model, and evaluating the R^2 value elucidates the correlation

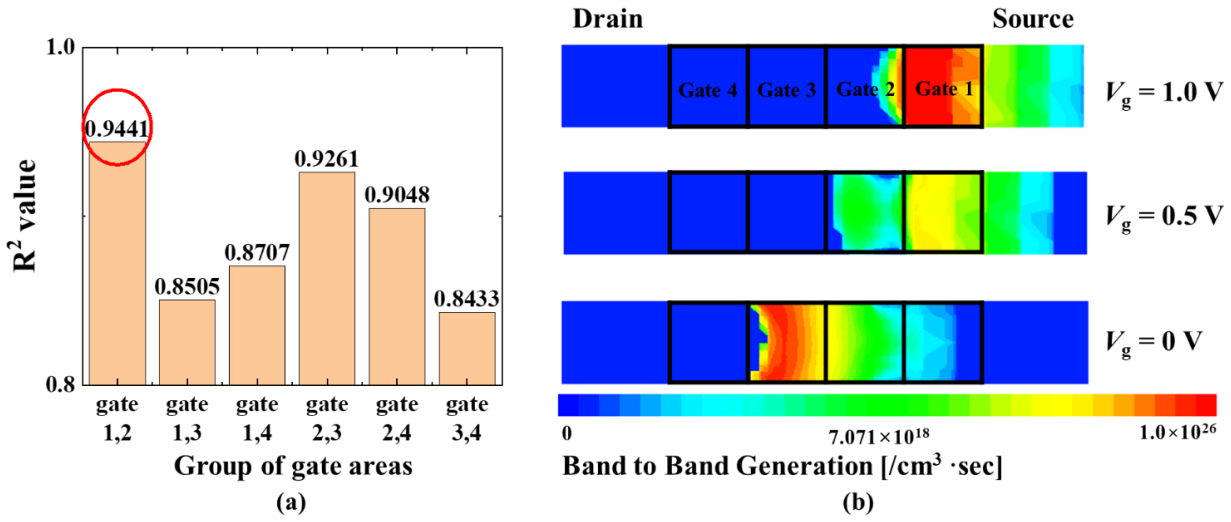

Fig. 4. (a) R^2 value of each gate areas; (b) Electron BTBT generation of channel and separated gate area.

between V_{on} and the group.

Sixteen parameters from the gates and eight parameters from the conduction and valence bands in the energy diagram were selected as input, while two parameters (V_{on}, V_{th}) were designated as the output. The dense layer architecture was configured as 24 - 16 - 8 - 2, utilizing the ReLU function [25]. The ADAM optimizer was employed for precise error correction, with a learning rate set to 0.001.

The comparison of R^2 values among different gate groups revealed that gate 1 and gate 2 exhibit a substantial correlation with V_{on}, as depicted in Fig. 4(a). Notably, the group containing gate 2 demonstrated R^2 values consistently at or above 0.9, indicating a robust correlation with V_{on}. This outcome highlights the significant influence of gate 2 on V_{on}. Considering that a significant portion of current in TFET is attributed to BTBT, as illustrated in Fig. 4(b) for an approximate gate voltage (V_g = 0.5 V) estimating V_{on}, BTBT primarily occurs at gate 1 and gate 2. This method enables the identification of the relative area contributing to the effect. The results confirm that ML models can effectively discern causative factors, facilitating optimization by establishing associ ations with each parameter.

IV. Multiple Causes of Variation

To validate the previously developed ML model, it is crucial to examine whether it accounts for various effects. In contrast to MOSFETs, TFETs have been shown to receive inversion carriers from the drain. This inversion charge inhibits channel band bending, a phenomenon influenced by randomly distributed metal grains in the gate [26]. Additionally, when the V_d is low, several additional phenomena come into play. These include ambipolar characteristics, directly influenced by BTBT, and super-linear onset, observable by examining ambipolar current (I_{AMB}), V_{th}, and V_{on} [27].

The ML model for this investigation derived input from the structure and energy diagram, similarly shown as in Section 2. However, the output parameters were derived from Fig. 5(a) (I_d-V_g curve when V_d = 0.1 V). The selected output parameters for the ML model were I_{AMB}, V_{th}, and V_{on}, with I_{AMB} measured when V_g = -1 V. The built model exhibited a high R^2 value for predictions at each parameter, as shown in Fig. 5(b)-(d). The R^2 values for each parameter— I_{AMB} (0.9901), V_{th} (0.9901), and V_{on} (0.9927)—demonstrate that the ML model can accurately predict various phenomena with a high level of confidence.

V. Prediction of Exceptional Situation

While most device structures exhibit average performance, devices such as CMOS or static random access memory (SRAM) can face performance challenges in exceptional situations [28]. This paper leverages ML to predict and address such exceptional scenarios that deviate significantly from the norm. ML

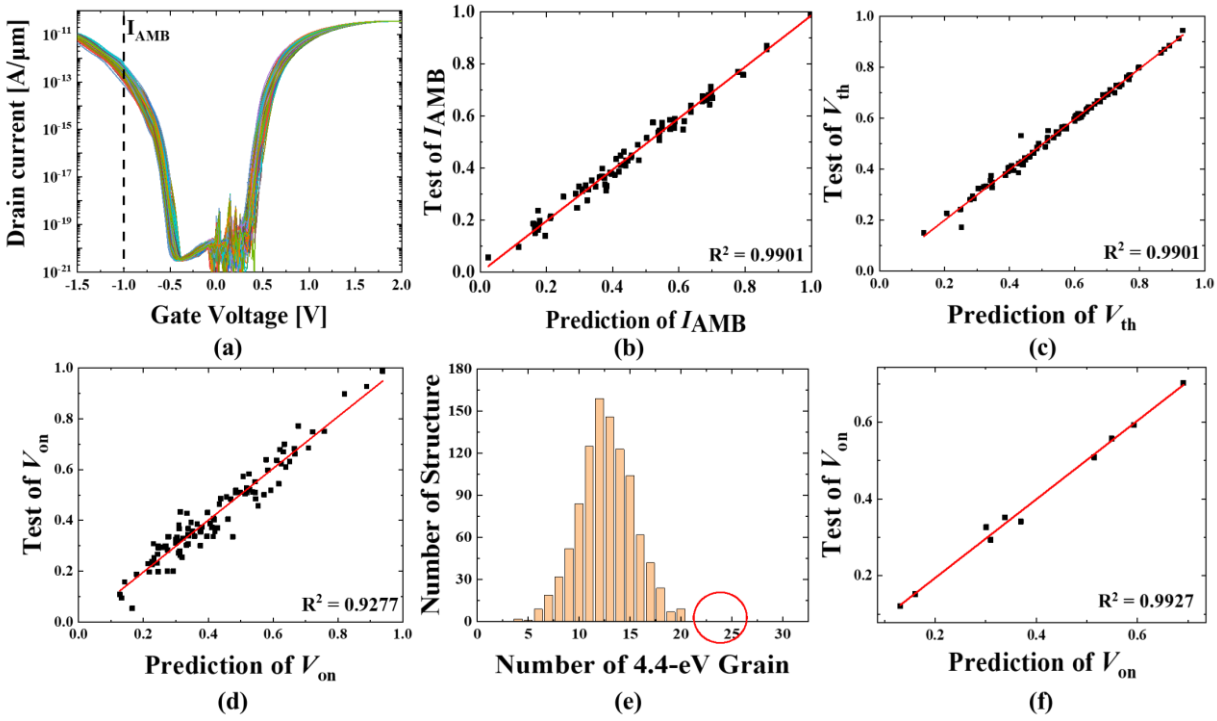

Fig. 5. (a) I_d-V_g curve of nanowire TFET at V_d = 0.1 V; (b) R^2 value of I_{AMB}; (c) R^2 value of V_{th}; (d) R^2 value of V_{on}; (e) Number of 4.4-eV grains; (f) R^2 value of prediction of V_{on} and test V_{on} of new 10 exceptional data.

models, developed in Section 2 and Section 5, were trained using data from Fig. 5(e).

Each gate in the ML model comprises grains with a 40% probability, featuring 4.4-eV grains whereas typical structures consist of 12 to 13 (average of 12.678) grains. To simulate an exceptional situation, 10 new structures were created, each with a 75% probability of acquiring 4.4-eV grains. In the existing structures, several 4.4-eV grains were located at positions 26, 22, 24, 20, 27, 24, 24, 26, 20, and 26, typically situated in the red part of Fig. 5(e). These structures were not part of the ML model training.

To make predictions, the grains and energy diagram of the structures were normalized using MinMaxScaler, a process consistent with the existing ML model inputs. The prediction of the input and output of the ML model was also normalized. Comparing the predicted V_{on} with the actual results, a high R^2 value of 0.9927 was achieved [Fig. 5(f)]. This outcome demonstrates that the ML model can effectively predict various exceptional situations.

VI. Conclusions

This study proposes the optimization of the ML model to establish a correlation between WFV and the variation of V_{on} in TFETs. Through the optimization and analysis of the ML model, it becomes evident that TFET performance is more affected by the number of gate regions than by the entire grain structure of the gate. This implies that only a few grains exhibit a high correlation with TFET's V_{on}. The ML model, relying on diverse data and exhibiting a strong dependence on parameters like V_d, demonstrates the potential for identifying multiple influencing factors. Furthermore, the ML model predicts that a gate with a higher proportion of 4.4 eV WF is likely to provide insights into the underlying causes. Ultimately, the results indicate the potential for prediction and analysis in the semiconductor process or simulation, particularly with sufficient and diverse data.

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REFERENCES

[1] C.-T. Sah, "Characteristics of the metal-oxide-semiconductor transistors," *IEEE Trans. Electron Devices*, Vol. 11, No. 7, pp. 324-345, 1964.

[2] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Electron Device Lett.*, Vol. 27, No. 4, pp. 297-300, 2006.

[3] J. H. Kim, S. Kim, and B.-G. Park, "Double-gate TFET with vertical channel sandwiched by lightly doped Si," *IEEE Trans. Electron Devices*, Vol. 66, No. 4, pp. 1656-1661, 2019.

[4] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, Vol. 98, No. 12, pp. 2095-2110, 2010.

[5] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "Vertical Si-Nanowire $ n $-Type Tunneling FETs With Low Subthreshold Swing (≤ 50 [mV/decade] at Room Temperature," *IEEE Electron Device Lett.*, Vol. 32, No. 4, pp. 437-439, 2011.

[6] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, Vol. 28, No. 8, pp. 743-745, 2007.

[7] N. Damrongplasit, C. Shin, S. H. Kim, R. A. Vega, and T.-J. K. Liu, "Study of random dopant fluctuation effects in germanium-source tunnel FETs," *IEEE Trans. Electron Devices*, Vol. 58, No. 10, pp. 3541-3548, 2011.

[8] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Electron Devices*, Vol. 50, No. 5, pp. 1254-1260, 2003.

[9] J. H. Kim, H. W. Kim, Y. S. Song, S. Kim, and G. Kim, "Analysis of current variation with work function variation in l-shaped tunnel-field effect transistor," *Micromachines*, Vol. 11, No. 8, p. 780, 2020.

[10] K. M. Choi, S. K. Kim, and W. Y. Choi, "Influence of number fluctuation and position variation of channel dopants and gate metal grains on tunneling field-effect transistors (TFETs)," *J. Nanosci. Nanotechnol.*, Vol. 16, No. 5, pp. 5255-5258, 2016.

[11] Y.-C. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *J. Appl. Phys.*, Vol. 92, No. 12, pp. 7266-7271, 2002.

[12] H. Nam and C. Shin, "Study of high-k/metal-gate work-function variation using Rayleigh distribution," *IEEE Electron Device Lett.*, Vol. 34, No. 4, pp. 532-534, 2013.

[13] G. Kim, J. H. Kim, J. Kim, and S. Kim, "Analysis of work-function variation effects in a tunnel field-effect transistor depending on the device structure," *Appl. Sci.*, Vol. 10, No. 15, p. 5378, 2020.

[14] C. C. Hobbs *et al.*, "Fermi-level pinning at the polysilicon/metal-oxide interface-Part II," *IEEE Trans. Electron Devices*, Vol. 51, No. 6, pp. 978-984, 2004.

[15] A. Ravindran, A. George, C. S. Praveen, and N. Kuruvilla, "Gate all around nanowire TFET with high ON/OFF current ratio," *Mater. Today Proc.*, Vol. 4, No. 9, pp. 10637-10642, 2017.

[16] Y. Lee, H. Nam, J.-D. Park, and C. Shin, "Study of work-function variation for high- κ metal-gate Ge-Source tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2143-2147, 2015.

[17] H. F. Dadgour, K. Endo, V. K. De, and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors—Part II: Implications for process, device, and circuit design," *IEEE Trans. Electron Devices*, Vol. 57, No. 10, pp. 2515-2525, 2010.

[18] T. M. Mitchell and T. M. Mitchell, *Machine learning*, vol. 1, no. 9. McGraw-hill New York, 1997.

[19] J. Lim and C. Shin, "Machine learning (ML)-based model to characterize the line edge roughness (LER)-induced random variation in FinFET," *IEEE Access*, Vol. 8, pp. 158237-158242, 2020.

[20] Y. S. Bankapalli and H. Y. Wong, "TCAD augmented machine learning for semiconductor device failure troubleshooting and reverse engineering," in *2019 International Conference on*

Simulation of Semiconductor Processes and Devices (SISPAD), 2019, pp. 1-4.

[21] Y.-C. Wu and Y.-R. Jhan, "Introduction of synopsys sentaurus TCAD simulation," in *3D TCAD Simulation for CMOS Nanoeletronic Devices*, Springer, 2018, pp. 1-17.

[22] E. P. Gyftopoulos and J. D. Levine, "Work function variation of metals coated by metallic films," *J. Appl. Phys.*, Vol. 33, No. 1, pp. 67-73, 1962.

[23] G.-B. Huang, "Learning capability and storage capacity of two-hidden-layer feedforward networks," *IEEE Trans. neural networks*, Vol. 14, No. 2, pp. 274-281, 2003.

[24] Z. Zhang, "Improved adam optimizer for deep neural networks," in *2018 IEEE/ACM 26th International Symposium on Quality of Service (IWQoS)*, 2018, pp. 1-2.

[25] A. F. Agarap, "Deep learning using rectified linear units (relu)," *arXiv Prepr. arXiv1803.08375*, 2018.

[26] H. W. Kim and J. H. Kim, "Study on the Influence of Drain Voltage on Work Function Variation Characteristics in Tunnel Field-effect Transistor," *J. Semicond. Technol. Sci.*, Vol. 20, No. 6, pp. 558-564, 2020.

[27] L. De Michielis, L. Lattanzio, and A. M. Ionescu, "Understanding the superlinear onset of tunnel-FET output characteristic," *IEEE Electron Device Lett.*, Vol. 33, No. 11, pp. 1523-1525, 2012.

[28] K. Bernstein, R. K. Cavin, W. Porod, A. Seabaugh, and J. Welser, "Device and architecture outlook for beyond CMOS switches," *Proc. IEEE*, Vol. 98, No. 12, pp. 2169-2184, 2010.

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